

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30585/7	SERIAL NO. 09/330,852
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		APPLICANT David L. Reese, et al.	# 2
		FILING DATE June 11, 1999	GROUP ART UNIT 2705 2124

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	3,781,823	12/25/73	Senese	340	172.5	July 28, 1972
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	4,455,602	06/19/84	Baxter	364	200	May 22, 1981
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	5,638,525	06/10/97	Hammond	395	385	Feb. 10, 1995
	5,796,939	8/18/98	Berc, et al.	395	184.01	Mar. 10, 1997
	5,802,272	9/1/98	Sites, et al.	395	183.21	Dec. 19, 1994
	5,822,578	10/13/98	Frank	395	591	June 5, 1995
	5,832,205	11/03/98	Kelly	395	185.06	Aug. 20, 1996
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						YES NO
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<b>INFORMATION DISCLOSURE CITATION</b> (Use several sheets if necessary)		APPLICANT David L. Reese, et al.	
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		Raymond J. Hookway, et al., Combining Emulation and Binary Translation (August 28, 1997) <a href="http://www.digital.com/info/DTJP01HM.HTM">http://www.digital.com/info/DTJP01HM.HTM</a>
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*Chu, Q*

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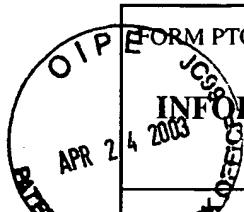
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EXAMINER <i>Chris G.</i>	DATE CONSIDERED <i>4-15-04</i>
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<b>INFORMATION DISCLOSURE CITATION</b>  (Use several sheets if necessary)		APPLICANT David L. Reese, et al.			
		FILING DATE June 11, 1999	GROUP ART UNIT 2703 2124		
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Papers, Etc.)</b>					
<p><i>Not Considered</i></p> <p><i>On P.E. JES</i></p> <p><i>NOV 19 1999</i></p> <p><i>U.S. PATENT &amp; TRADEMARK OFFICE</i></p> <p>T.M. Conte, et al., "Using branch handling hardware to support profile-driven optimization," Proceedings of the 27<sup>th</sup> Annual International Symposium on Microarchitecture San Jose, CA (Dec. 1994)</p> <p>J.S. Cox et al., "Commercializing profile-driven optimization." Proceedings of the 28<sup>th</sup> Hawaii International Conference on System Sciences, vol. 1 Maui, HI, pp. 221-228 (Jan. 1995)</p> <p>Digital Equipment Corp., White Paper: How DIGITAL FX!32 Works (September 1997) <a href="http://www.digital.com/semiconductor/amt/fx32/fx-white.htm">http://www.digital.com/semiconductor/amt/fx32/fx-white.htm</a></p> <p>Ebciooglu and Altman, IBM Research Report, DAISY: Dynamic Compilation for 100% Architectural Compatibility, IBM Research Division (1996)</p> <p>Linda Geppert et al., Transmeta's Magic Show, IEEE Spectrum, vol. 37 no. 5, pp. 26-33 (May 2000)</p> <p>Ronald M. Guffin, Microdiagnostics for the Standard Computer MLP-900 Processor, IEEE Transactions on Computers, Vol. C-20 No. 7, pp. 803-808 (July 1971)</p> <p>Linley Gwennap, MDR Technical Library Special Report, Intel's Merced and IA-64 Technology and Market Forecast, IA-64 Software Model - Chapter 3 excerpt Microprocessor Report, MicroDesign Resources (July 20, 1998)</p> <p>Linley Gwennap, MDR Technical Library Special Report, Intel's Merced and IA-64: Technology and Market Forecast, Executive Summary, Microprocessor Report, MicroDesign Resources (July 20, 1998)</p> <p>Linley Gwennap, First Merced Patent Surfaces, Intel Document Reveals Processors With Dual Instruction Sets, Microprocessor Report, MicroDesign Resources (July 20, 1998)</p> <p>R.E. Hank, et al., Proceeding of the 28<sup>th</sup> Annual International Symposium on Microarchitecture, pp. 158-168 (Dec. 1995)</p> <p>Raymond J. Hookway, et al., Combining Emulation and Binary Translation (August 28, 1997) <a href="http://www.digital.com/info/DTJP01HM.HTM">http://www.digital.com/info/DTJP01HM.HTM</a></p> <p>Harold W. Lawson, Jr., et al., Functional Characteristics of a Multilingual Processor, IEEE Transactions on Computers, Vol. C-20, No. 7, pp. 732-742 (July, 1971)</p> <p>K.N.P. Menezes, "Hardware-based profiling for program optimization," Ph.D. thesis, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, North Carolina (1997)</p> <p>Nanodata Corporation, QM-1 Hardware level User's Manual (1975)</p> <p>Nanodata Corporation, QM-2 Processor (1976)</p> <p>Robert F. Rosin, Contemporary Concepts of Microprogramming and Emulation, Computing Surveys, Vol. 1 No. 4, pp. 197-212 (December 1969)</p> <p><i>Not Considered</i></p> <p>Robert F. Rosin, An Environment for Research in Microprogramming and Emulation, Communications of the ACM, Vol. 15 No. 8, pp. 748-760 (August 1972)</p>					
EXAMINER <i>Chris J.</i>		DATE CONSIDERED <i>4-15-04</i>			

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		FILING DATE June 11, 1999	GROUP ART UNIT 2765 2124
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Papers, Etc.)</b> <p>Not ↓ N.T. Confidential</p> <p>NOV 13 2000 U.S. PATENT &amp; TRADEMARK OFFICE O I P E J C B S</p> <p>Standard Computer Corp., IC-9000 Central Processing Unit - Principles of Operation (undated - possibly 1969)</p> <p>W.T. Wilner, Design of the Burroughs B1700, Fall Joint Computer Conference, pp. 489-497 (1972)</p> <p>W.T. Wilner, Burroughs B1700 Memory Utilization, Fall Joint Computer Conference, pp. 579-586 (1972)</p>			
<p>RECEIVED NOV -7 2000 TC 2100 MAIL ROOM</p>			
EXAMINER <i>Ch, Q</i>	DATE CONSIDERED <i>4-15-04</i>		





U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

**INFORMATION DISCLOSURE CITATION**

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ATTY. DOCKET NO.  
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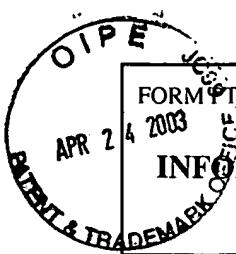
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	4,575,797	03/11/1986	Gruner	364	200	May 22, 1981
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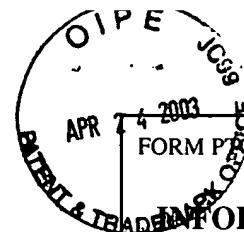
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<i>Chris J.</i>	<i>4-15-04</i>